Amendments to the Claims

This listing of claims will replace all prior version, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A method for providing an improved integrated circuit device comprising the steps of:

providing active and passive areas in the substrate,

providing a plurality of slots in the substrate after providing the active and passive areas,

oxidizing the plurality of slots;

providing metal in each of the plurality of slots,

providing a dielectric coating over the slots;

providing etched contacts in select areas remote from the location of the slots;

providing an additional layer of metal that interconnects the etched contacts and the ~~buried~~ metal in the slots in select areas around the etched contacts, resulting in metal of three levels; and

providing one level of the metal on a top surface in the substrate and two levels of the metal comprise**ing** a buried power buss (BPB).

2. (currently amended) The method of claim 1 wherein the providing steps comprise**ing** the step of providing three independent oxide isolated metal layers being of sufficient thickness to carry high current.

3. (cancelled)

4. (cancelled)

5. (cancelled)

6. (original) The method of claim 1 wherein active and passive areas are provided for bipolar, CMOS, BICMOS, DMOS and BCD technologies with improved properties.

7. (previously presented) The method of claim 1 wherein select slots are opened in the substrate prior to metal to allow the oxide to be removed from the bottom of slots that are to make ground contact to the substrate and metal contact to the buried metal to replace a sinker.

8. (cancelled)

9. (previously presented) The method of claim 1 wherein three layers of metal are provided with only one layer of metal requiring masking and pattern etching.

10. (cancelled)

11. (cancelled)

12. (cancelled)

13. (previously presented) The method of claim 1 whereby the slots are located to

provide significant circuit advantages for the various technologies.

14. (cancelled)

15. (cancelled)

16. (original) The method of claim 1 whereby three layers of isolated metal interconnect are formed while only requiring one layer of dielectric to be deposited and contact etched, versus standard triple metal processes which requires three layers of dielectric to be deposited and contact (or via) etched.

17. (cancelled)

18. (currently amended) The method of claim ~~1~~ 2 whereby ~~the~~ a high current is carried on the buried power buss (BPB) and ~~the~~ a third layer is for interconnection of low power circuitry.

19. (cancelled)